AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth below. A listing of all pending claims is presented below.

1. (amended) A clock switching circuit for receiving as an input a plurality of clock signals including a first clock signal and a second clock signal[s] and switching [one] an output clock signal to be output from said first clock signal to said second clock signal, comprising:

a plurality of unit circuits for respectively receiving as an input at least said first and said second clock signals, associated selection signals of the first and second clock signals, and an enabling signal[s] [and] controlling supplying and stopping of said first and second clock signals in accordance with said selection signals and said enabling signal[s]; [and]

a feedback circuit for monitoring output conditions of said plurality of unit circuits and, when outputting of all clock signals of said plurality of unit circuits [was] is stopped as a result of stopping said first clock signal, [giving] providing said enabling signal to the [a] plurality of said unit circuits [said enabling signals for approving] enabling starting of a supply of said second clock signal; and

an output circuit at a final stage connected to all outputs of said plurality of unit circuits for outputting any one of said plurality of clock signals output from said plurality of unit circuits; and

wherein said output circuit at the final stage comprises a discharge portion for discharging an output side node of the output circuit in accordance with said enabling signal.

2. (currently amended) [A] The clock switching circuit as set forth in claim 1, wherein each of said plurality of unit circuits comprises a delay unit for delaying timing of changing a voltage level indicating a supplying condition of said first clock signal to a voltage level indicating a stopping condition of a monitor signal used for monitoring said output condition when an instruction of stopping said first clock signal is given by said selection signal, and delaying an operation of starting a supply of the second clock signal by using a point that said enabling signal becomes active as a starting point when an instruction of starting a supply of said second clock signal is given by said selection signal.

3. (currently amended) [A] The clock switching circuit as set forth in claim [1] 2, wherein:

each of said plurality of unit circuits further comprises a clock output gate unit, whose operation timing is controlled by said delay unit, for stopping or starting outputting of [input] said clock signal; and

said delay unit and said clock output gate unit operate in synchronization with said [input] clock signal.

4. (currently amended) [A] The clock switching circuit as set forth in claim 1, further comprising:

an output circuit at a final stage connected to all outputs of said plurality of unit circuits for outputting any one of said plurality of clock signals output from said plurality of unit circuits; and

a plurality of synchronization portions provided at an input stage for said selection signal in each of said plurality of unit circuits for operating in synchronization with a clock signal output from said output circuit to unify phases of said selection signals of said plurality of unit circuits.

5. (currently amended) [A] The clock switching circuit as set forth in claim [1] 2, wherein:

said delay unit operates in synchronization with said [input] clock signal, and further comprising

a synchronization portion provided at an input stage of said delay unit in each of said plurality of unit circuits for operating in synchronizing with said [input] clock signal.

6. Canceled

7. (Newly-added) The clock switching circuit as set forth in claim 1, wherein said first clock signal and said second clock signal are included in said plurality of clock signals as said input.

8. (newly added) The clock switching circuit as set forth in claim 1, wherein said first clock signal and said second clock signal are selected from said plurality of clock signals.

9. (newly-added) The clock switching circuit as set forth in claim 1, wherein said first clock signal and said second clock signal have different frequencies and phases, said switching occurring while preventing generation of a hazard.

10. (newly-added) The clock switching circuit as set forth in claim 1, wherein said plurality of clock signals includes signals having different frequencies and phases.

11. (newly-added) The clock switching circuit, comprising:

an input circuit for receiving as an input a plurality of clock signals including a first clock signal and a second clock signal for switching an output clock signal from said switching circuit to be output from said first clock signal to said second clock signal;

a plurality of unit circuits respectively associated with said input circuit receiving as an input at least said first and said second clock signals, associated selection signals of the first and second clock signals, and an enabling signal controlling supplying and stopping of said first and second clock signals in accordance with said selection signals and said enabling signal wherein each of said plurality of unit circuits comprises a delay unit for delaying timing of changing a voltage level indicating a supplying condition of said first clock signal to a voltage level indicating a stopping condition of a monitor signal used for monitoring said output condition when an instruction of stopping said first clock signal is given by said selection signal, and

delaying an operation of starting a supply of the second clock signal by using a point that said enabling signal becomes active as a starting point when an instruction of starting a supply of said second clock signal is given by said selection signal;

means for monitoring output conditions of said plurality of unit circuits and, when outputting of all clock signals of said plurality of unit circuits is stopped as a result of stopping said first clock signal, providing said enabling signal to said plurality of said unit circuits enabling starting of a supply of said second clock signal; and

an output circuit at a final stage connected to all outputs of said plurality of unit circuits for outputting any one of said plurality of clock signals output from said plurality of unit circuits.

12. (newly added)The clock switching circuit as set forth in claim 11, wherein said output circuit at the final stage comprises a discharge portion for discharging an output side node of the output circuit in accordance with said enabling signal.

13. (newly added) The clock switching circuit as set forth in claim 11, wherein:

each of said plurality of unit circuits further comprises a clock output gate unit, whose operation timing is controlled by said delay unit, for stopping or starting outputting of said clock signal; and

said delay unit and said clock output gate unit operate in synchronization with said clock signal.

14. (newly-added) The clock switching circuit as set forth in claim 11, further comprising:

an output circuit at a final stage connected to all outputs of said plurality of unit circuits for outputting any one of said plurality of clock signals output from said plurality of unit circuits; and

a plurality of synchronization portions provided at an input stage for said selection signal in each of said plurality of unit circuits for operating in synchronization with a clock signal output from said output circuit to unify phases of said selection signals of said plurality of unit circuits.

15. (newly added) The clock switching circuit as set forth in claim 11, wherein:

said delay unit operates in synchronization with said clock signal, and further comprising

a synchronization portion provided at an input stage of said delay unit in each of said plurality of unit circuits for operating in synchronizing with said clock signal.

16. (newly added) The clock switching circuit as set forth in claim 11, wherein said first clock signal and said second clock signal are included in said plurality of clock signals as said input.

17. (newly-added) The clock switching circuit as set forth in claim 11, wherein said first clock signal and said second clock signal are selected from said plurality of clock signals.

18. (newly-added) The clock switching circuit as set forth in claim 11, wherein said first clock signal and said second clock signal have different frequencies and phases, said switching occurring while preventing generation of a hazard.

19. (newly-added) The clock switching circuit as set forth in claim 11, wherein said plurality of clock signals includes signals having different frequencies and phases.

20. (New) The clock switching circuit as set forth in claim 11 wherein said delay unit delays actual clock stopping from an instruction for clock stopping by a predetermined clock cycle and actual starting of a clock supply for a clock supply approach predetermined by a clock cycle.